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APPLICATION FOR LETTERS PATENT

**Methods of Forming Semiconductor Stacked Die  
Devices**

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1      **RELATED APPLICATION**

2      This application is a divisional application of and claims priority to U.S.  
3      Patent Application Serial No. 09/679,143, filed on October 3, 2000, the disclosure  
4      of which is incorporated by reference herein.

5

6      **TECHNICAL FIELD**

7      This invention relates to generally to method of forming semiconductor  
8      devices and, more particularly to method of forming semiconductor stacked die  
9      constructions.

10

11      **BACKGROUND**

12      Semiconductor devices are typically constructed from a silicon or gallium  
13      arsenide wafer through a process involving a number of deposition, masking,  
14      diffusion, etching, and implanting steps. Usually, many individual devices are  
15      constructed on the same wafer. After fabrication, the wafer is typically sawed or  
16      otherwise singulated into individual units, where each unit takes the form of an  
17      integrated circuit (IC) die.

18      It has become a practice in the industry to provide integrated circuit  
19      devices in the form of so-called "stacked die" arrangements. Stacked die  
20      arrangements typically involve two or more IC die that are fixed upon one another,  
21      typically through some type of adhesive arrangement. Interconnections can then  
22      be made between the individual die to provide an overall device with a desirable  
23      density and enhanced functionality.

24      Examples of stacked die arrangements are described in detail in the  
25      following U.S. Patents, to which the reader is referred for additional detail: U.S.

1 Patent Nos. 5,291,061; 6,051,886; 5,397,916; 5,434,745; 6,093,939; and  
2 5,864,177.

3 To date, interconnections between the individual die of stacked die  
4 arrangements have been made at or near the periphery of each die. U.S. Patent  
5 Nos. 5,291,061, and 5,397,916 provide very good examples of this type of  
6 interconnection. As device processing speeds continue to increase, those involved  
7 in the design of semiconductor devices are necessarily forced to consider and  
8 reconsider traditionally accepted notions of circuit design. One particular area of  
9 interest in the industry concerns the design and fabrication of memory devices,  
10 and particularly those memory devices that employ stacked die arrangements.

11 Accordingly, this invention arose out of concerns associated with providing  
12 improved systems that employ stacked die arrangements, and methods of forming  
13 the same.

14

15 **SUMMARY**

16 Semiconductor devices and methods of forming semiconductor devices are  
17 described. In one embodiment, a method comprises forming at least one  
18 conductive structure within a plurality of semiconductor substrates, said act of  
19 forming comprising first forming said at least one conductive structure to extend  
20 into a respective semiconductor substrate a distance that is less than an elevational  
21 thickness of the substrate, and second removing substrate material elevationally  
22 adjacent said one conductive structure effective to expose a surface of said one  
23 conductive structure, at least portions of one of the conductive structures having  
24 oppositely facing, exposed outer surfaces; and stacking individual substrates  
25

1 together such that individual conductive structures on each substrate are in  
2 electrical contact with the conductive structures on a next adjacent substrate.

3 In another embodiment, a method comprises forming at least one  
4 conductive structure within each of a plurality of semiconductor substrates, said at  
5 least one conductive structure comprising a multi-layered structure formed  
6 through successive depositions and etchings and having oppositely-facing  
7 surfaces; exposing portions of each oppositely-facing surface on at least one of the  
8 substrates; and processing the substrates sufficient to form electrical connections  
9 between the substrates, said processing comprising stacking the substrates on one  
10 another so that the conductive structures on adjacent substrates are electrically  
11 connected.

12 In another embodiment, a method comprises forming at least one  
13 conductive structure within each of a plurality of semiconductor substrates, each  
14 conductive structure having oppositely-facing surfaces; after said forming,  
15 exposing portions of at least one oppositely-facing surface on at least one of the  
16 substrates, said exposing comprising etching portions of said at least one substrate  
17 to expose said at least one surface; and processing the substrates sufficient to form  
18 electrical connections between the substrates by stacking the substrates on one  
19 another so that electrical connection can be made between conductive structures  
20 on adjacent substrates, said processing comprising: forming additional conductive  
21 material over and in electrical contact with said exposed portions; and bonding at  
22 least some of the additional conductive material on one substrate with additional  
23 conductive material on another of the substrates.

24 In a further embodiment, a method comprises forming at least one multi-  
25 layered, conductive pad structure within each of a plurality of semiconductor

1 substrates, each conductive pad structure having oppositely-facing surfaces;  
2 exposing portions of each oppositely-facing surface on at least one of the  
3 substrates, at least one oppositely-facing surface being exposed by etching  
4 portions of said at least one substrate to expose said at least one surface; and after  
5 said exposing, forming additional conductive material over and in electrical  
6 contact with said exposed portions by plating more than one additional conductive  
7 material over said exposed portions.

8 In yet another embodiment, a method comprises a step for providing a  
9 multi-layered structure within a plurality of substrates, the multi-layered structures  
10 having a front side and a back side; a step for thinning at least one of the substrates  
11 after providing the multi-layered structure; a step for exposing portions of the back  
12 side of said at least one substrate that was thinned; a step for forming additional  
13 conductive material over and in electrical contact with the multi-layered structure  
14 of the substrate that was thinned; and a step for stacking the substrates such that  
15 the multi-layered structures with the substrates are in electrical contact with one  
16 another.

17

18 **BRIEF DESCRIPTION OF THE DRAWINGS**

19 Fig. 1 is a diagrammatic side sectional view of a semiconductor wafer  
20 fragment, in process, in accordance with the described embodiment.

21 Fig. 2 is diagrammatic side sectional view of the Fig. 1 wafer fragment, in  
22 process, in accordance with the described embodiment.

23 Fig. 3 is a diagrammatic side sectional view of the Fig. 2 wafer fragment, in  
24 process, in accordance with the described embodiment.

1       Fig. 4 is a diagrammatic side sectional view of the Fig. 3 wafer fragment, in  
2 process, in accordance with the described embodiment.

3       Fig. 5 is a diagrammatic side sectional view of two exemplary substrates  
4 mounted in a stacked die arrangement in accordance with the described  
5 embodiment.

6       Fig. 6 is a diagrammatic side sectional view of four exemplary substrates  
7 mounted in a stacked die arrangement in accordance with the described  
8 embodiment.

9       Fig. 7 is a diagrammatic side sectional view of the Fig. 6 wafer fragment, in  
10 process, in accordance with the described embodiment.

11

12 **DETAILED DESCRIPTION**

13       **Exemplary Embodiment**

14       Fig. 1 shows a semiconductor wafer, in process, generally at 10 and  
15 includes a semiconductor substrate 12. In the context of this document, the term  
16 "semiconductor substrate" is defined to mean any construction comprising  
17 semiconductive material, including, but not limited to, bulk semiconductive  
18 materials such as a semiconductive wafer (either alone or in assemblies  
19 comprising other materials thereon) and semiconductive material layers (either  
20 alone or in assemblies comprising other materials). The term "substrate" refers to  
21 any supporting structure including, but not limited, to the semiconductive  
22 substrates described above.

23       Substrate 12 includes regions 14 that are fabricated to contain or comprise  
24 integrated circuit (IC) devices. In a preferred implementation, the integrated  
25 circuit devices comprise memory devices. One type of exemplary memory device

1 is a dynamic random access memory (DRAM) device, such as DRAM devices  
2 designed by the assignee of this document. It is to be understood, however, that  
3 this constitutes but one exemplary type of integrated circuit device that can be  
4 provided. Other types of integrated circuit devices (and not necessarily memory  
5 devices) can be provided without departing from the spirit and scope of the  
6 claimed subject matter.

7 A pair of regions 16 are shown and comprise interface regions that are  
8 designed to provide an interface between the integrated circuit devices within  
9 regions 14 and other circuitry that is external of the substrate 12.

10 A conductive structure 18 is formed within and supported by substrate 12.  
11 The exemplary structure 18 can comprise any suitable type of conductive structure  
12 and is positioned to make electrical contact with regions 16, and other conductive  
13 structures that will ultimately electrically connect the integrated circuit devices to  
14 the outside world, as will become apparent below. In a preferred implementation,  
15 conductive structure 18 comprises a multi-layered pad structure that is fabricated  
16 during processing of the devices in regions 14. The pad structure preferably  
17 comprises aluminum and can be formed through successive deposition/etching (or  
18 removal) steps.

19 The conductive structure can be formed at any suitable location within the  
20 substrate. It is desirable, however, to have the conductive structure formed at a  
21 substrate location that is not at the periphery of the substrate. This is because the  
22 conductive structure is going to be used to form electrical connections with other  
23 similar conductive structures on other substrates. These substrates will be  
24 mounted together in a stacked arrangement so that adjacent substrates are  
25 electrically connected through the conductive structures. The manner in which

1 these electrical connections is to be made desirably eliminates the need to make  
2 such electrical connections between the substrates at the periphery of, and external  
3 to the substrates, as will become apparent below. In the illustrated example, the  
4 conductive structure is disposed within the center of the substrate.

5 An insulative layer 20 is formed over substrate 12 and patterned to expose a  
6 front side 18a of conductive structure 18 as shown.

7 Referring to Fig. 2, wafer 10 is processed to remove a portion of the back  
8 side of the wafer, thus thinning the wafer. The wafer can be thinned through the  
9 use of any suitable techniques. For example, the wafer can be mechanically (or  
10 chemically-mechanical) abraded or polished to achieve the desired thinned wafer.

11 Referring to Fig. 3, portions of the wafer are removed, as by any suitable  
12 processing technique, sufficient to expose at least a portion of backside 18b of  
13 conductive structure 18. In the illustrated example, material of the wafer can be  
14 selectively etched, relative to the material from which the conductive structure 18  
15 is formed, so that the back side 18b of the conductive structure is exposed. Thus,  
16 at this point in the processing of wafer 12, conductive structure 18 has portions of  
17 both of its oppositely-facing surfaces exposed.

18 Referring to Fig. 4, additional conductive material 22, 24 is formed  
19 respectively, over and in electrical contact with the oppositely-facing surfaces (i.e.  
20 front side 18a and back side 18b) of conductive structure 18. In the illustrated and  
21 described embodiment, the conductive material is formed through known plating  
22 techniques. In this specific example, more than one conductive material is plated  
23 over the conductive structure 18. Specifically, a first conductive material 26, such  
24 as nickel, is first formed over the exposed surfaces of the conductive structure 18.  
25 Any suitable plating technique, e.g. electroless plating, can be used. After the first

1 conductive material 26 is plated over the exposed surfaces of the conductive  
2 structure 18, a second conductive material 28 is formed over and in electrical  
3 contact with first conductive material 26. Any suitable techniques can be used  
4 such as sputtering, evaporating, or plating to name a few. In the illustrated and  
5 described embodiment, second conductive material 28 comprises gold. The  
6 second conductive material can, however, comprise any suitable conductive  
7 material. For example, an alloy of tin and gold can be used. For purposes of  
8 further discussion, conductive material 22 will be referred to as the “top most”  
9 conductive material, and conductive material 24 will be referred to as the  
10 “bottommost” conductive material.

11 Notice that bottommost conductive material 24 is received entirely within  
12 an opening that is defined by a via that exposes the surface of the backside 18b of  
13 conductive structure 18. The reason for this will become apparent below.

14 It should be understood that while only one exemplary substrate is shown  
15 as being processed as described, in the preferred embodiment, multiple substrates  
16 are typically processed at one time so that they can be eventually joined or bonded  
17 together in a die stack.

18 Referring to Fig. 5, two exemplary substrates 12, 12a are shown. It will be  
19 appreciated that substrate 12a can be identical to or different from substrate 12.  
20 Substrates 12 and 12a are first moved into engagement with one another and then  
21 processed sufficiently such that a conductive bond forms between the bottommost  
22 conductive material of substrate 12 and the top most conductive material of  
23 substrate 12a. In one exemplary implementation, the conductive bond can be  
24 formed by stacking the substrates, either in wafer form or singulated die form, and  
25 then joining the conductive material on each of the substrates through ultrasonic

1 thermal compression. This is a good technique to use when the top- and  
2 bottommost conductive materials comprise gold. Other techniques can, of course,  
3 be used, e.g. thermal compression.

4 The Fig. 5 construction can thus comprise a first die 12 having IC devices  
5 thereon and a second die 12a also having IC devices thereon. Die 12, 12a are  
6 mounted together in a stacked arrangement such that the conductive structures of  
7 each die are in electrical contact with one another. Thus, the necessity for any  
8 such electrical contact to be made external of the substrates or die can be  
9 eliminated.

10 The above technique can be used to form any suitable number of individual  
11 dies into a stacked die arrangement. For example, Fig. 6 shows an arrangement of  
12 multiple stacked die that consists of four separate substrates (12-12c) that are  
13 joined together as described above. Notice that substrate 12c does not have both  
14 faces of its conductive structure 18 exposed.

15 Hence, the inventive techniques described above enable multiple substrates  
16 or die to be formed into a stacked arrangement, with operative electrical  
17 connections between the die being made by virtue of conductive structures that are  
18 disposed entirely within internal regions of the die. In one preferred embodiment,  
19 the conductive structures are formed so that they are generally disposed in the  
20 center of each die. It is to be appreciated, however, that the conductive structures  
21 can be formed at any suitable location on or within the individual die. In the  
22 illustrated and described embodiment, the collection of conductive structures for  
23 each die are disposed along a common line A.

24 Once the die have been formed into a stacked arrangement as described  
25 above, they can further processed into individual packages. For example, Fig. 7

1 shows the Fig. 6 die stack where an insulative layer 30 has been formed over the  
2 die stack. A conductive line 32 is provided and makes contact with conductive  
3 material 22 of the uppermost die 12. Multiple conductive pads 34 are provided  
4 over layer 30, with exemplary solder balls 36 being received over each of the pads  
5 34. Processing the die stack can now continue using conventional techniques to  
6 form an IC package, as will be appreciated and understood by those of skill in the  
7 art.

8 The various stacked die arrangements that can be formed through the  
9 inventive techniques described above are advantageous in that the connective  
10 distances as between the individual die can be drastically reduced over other  
11 constructions where connections are typically made at the periphery of the die.  
12 This is particularly advantageous in the field of memory devices, e.g. SDRAMs  
13 and the like, where, for performance purposes, it is highly desirable to reduce stub  
14 lengths to the shortest possible distances. In addition, the inventive techniques can  
15 enable increased package capacity while providing constructions that more easily  
16 dissipate heat. These constructions can more easily dissipate heat because the  
17 conductive material joining the individual die can act as a funneling mechanism  
18 for heat. Additionally, other material layers, e.g. non-conductive joining material  
19 can be formed on the die surfaces to provide not only mechanical support, but  
20 further assist in heat dissipation. In addition, the constructions that are provided  
21 by the inventive techniques can reduce the number of I/O connections per die.  
22 Other advantages will be apparent to those of skill in the art.

23 Although the invention has been described in language specific to structural  
24 features and/or methodological steps, it is to be understood that the invention  
25 defined in the appended claims is not necessarily limited to the specific features or

1 steps described. Rather, the specific features and steps are disclosed as preferred  
2 forms of implementing the claimed invention.

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